

ERASE VERIFY FOR NON-VOLATILE MEMORY

Technical Field of the Invention

[01] The present invention relates generally to memory devices and in particular the present invention relates to determining erase levels of memory cells in non-volatile memory devices.

Background of the Invention

[02] The use of non-volatile memory systems that maintain data integrity when a power supply is removed are expanding rapidly in integrated circuit technology. A class of non-volatile memory systems having memory cells which has a source, a drain, a channel, a floating gate over the channel and a control gate are widely used. Two popular types of non-volatile memory designs in this class is the electronically erasable and programmable read only memories (EEPROM) and the FLASH erasable-programmable read only memory (EPROM). The FLASH EPROM or flash memory system allows the simultaneous erasure of multiple memory cells.

[03] The floating gate of the memory cell stores data and the control gate of the memory cell controls the floating gate. The floating gates are generally formed from polysilicon members completely surrounded by an insulator. A memory cell is programmed when a charge is stored on the floating gate. Moreover, a memory cell is unprogrammed, or erased, when the charge is removed from the floating gate.

[04] One method of programming a memory cell is accomplished by applying a potential (e.g., 4-7 V) to its drain and a potential (e.g., 10-15 V) to its control gate ~~programs~~. This causes electrons to be transferred from the source to the floating gate of the memory cell. One method of erasing a memory cell is accomplished by applying a

Summary of the Invention

[09] The above-mentioned problems with memories and other problems are addressed by the present invention and will be understood by reading and studying the following specification.

[10] In one embodiment, a non-volatile memory comprises an array of non-volatile memory cells arranged in columns using bit lines, and a verify circuit selectively coupled to the bit lines to determine if the memory cells have a program level that is within a program level window defined by first and second reference signals.

[11] In another embodiment, a bit line verify system comprises a first comparator to compare a bit line current with a first reference current and produce a first output signal, and a second comparator to compare the bit line current with a second reference current and produce a second output signal.

[12] A memory device with an erase verify system is provided in yet another embodiment. The memory device comprises a memory array having a plurality of memory cells coupled to a bit line, a first comparator to compare a bit line voltage with a first reference voltage and produce a first output signal, and a second comparator to compare the bit line voltage with a second reference voltage and produce a second output signal.

[13] A non-volatile memory comprises an array of non-volatile memory cells arranged in columns using bit lines, and a verify circuit selectively coupled to the bit lines to determine if the memory cells have a program level that is within a program level window defined by first upper and second lower reference signals. Control circuitry is coupled to the verify circuit to determine that the memory cell is erased if the memory cell has a program level within the window. The control circuitry determines

that the memory cell is over-erased if the memory cell has a program level greater than the first upper reference signal. The control circuitry determines that the memory cell is under-erased if the memory cell has a program level lower than the second lower reference signal.

[14] A method of erase verifying a non-volatile memory cell is provided in one embodiment, the method comprises generating a first reference current, generating a second reference current, and comparing a bit line current from a column coupled to the non-volatile memory cell with the first reference current and the second reference current.

[15] A method of erase verifying a non-volatile memory cell is provided in another embodiment, the method comprises generating a first reference voltage, generating a second reference voltage, and comparing a bit line voltage from a column coupled to the non-volatile memory cell with the first reference voltage and the second reference voltage.

Brief Description of the Drawings

[16] Figure 1 is a simplified block diagram of a flash memory device of one embodiment of the present invention that is coupled to an external processor.

[17] Figure 2 is a schematic diagram of a memory array coupled to a verify circuit of one embodiment of the present invention.

[18] Figure 3 is a block diagram of a verify circuit of one embodiment of the present invention.

[19] Figure 4 is a block diagram of a verify circuit of one embodiment of the present invention.

[20] Figure 5 is a block diagram of another embodiment of a verify circuit of the present invention.

[21] Figure 6 is a block diagram of another embodiment of a verify circuit of the present invention.

[22] Figure 7 is a schematic diagram of a bit line current-to-voltage converter of one embodiment of the present invention.

[23] Figure 8 is a schematic diagram of a reference current-to-voltage converter of one embodiment of the present invention.

[24] Figure 9 is a schematic diagram of another embodiment of a reference current-to-voltage converter of the present invention.

[25] Figure 10 is a schematic diagram of a reference current-to-voltage converter of one embodiment of the present invention to provide multiple reference voltages.

Detailed Description of the Invention

[26] In the following detailed description of the preferred embodiments, reference is made to the accompanying drawings that form a part hereof, and in which is shown by way of illustration specific preferred embodiments in which the inventions may be practiced. These embodiments are described in sufficient detail to enable those skilled in the art to practice the invention, and it is to be understood that other embodiments may be utilized and that logical, mechanical and electrical changes may be made without departing from the spirit and scope of the present invention. The following detailed description is, therefore, not to be taken in a limiting sense, and the scope of the present invention is defined only by the claims.

[27] Figure 1 illustrates a block diagram of a flash memory device 100 that is coupled to an external processor 102. The memory device 100 has been simplified to

[28] focus on features of the memory that are helpful in understanding the present invention. The memory device 100 includes an array 116 of memory cells. The memory cells are preferably floating gate memory cells, and the array 116 is arranged in blocks of rows and columns. The blocks allow the memory cells to be erased in large groups. Data, however, is stored in the memory array 116 in small data groups (byte or group of bytes) and separate from the block structure. Erase operations are usually performed on a large number of cells in parallel.

[29] Address decode circuitry 112 is provided to decode address signals provided on address lines A0-Ax 114. Address signals are received and decoded to access the memory array 116. Data input and output buffer circuits 122 are included for bi-directional data communication over a plurality of data (DQ) lines 124 with the external processor 102. Control circuit 130 decodes signals provided on control lines 126 from the external processor 102. These signals are used to control the operations of the memory, including data read, data write, and erase operations, as known to those skilled in the art. Verify circuits 128 are included for verifying the state of a memory cell, as described in detail below.

[30] In addition, state machine(s) can be provided as part of the control circuitry to perform read, write and erase operations. The flash memory may also include a charge pump (not shown) that generates an elevated voltage, V_{pp} , used during programming of the memory cells and other internal operations. During write operations, V_{pp} is coupled to the memory cells for providing appropriate write operation programming power. Charge pump designs are known to those skilled in the art, and provide power which is dependent upon an externally provided supply of voltage V_{cc} .

[31] As stated above, the flash memory of Figure 1 has been simplified to facilitate a basic understanding of the features of the memory. Further, it will be appreciated that more than one flash memory can be included in various package

configurations. For example, flash memory cards can be manufactured in varying densities using flash memories.

[32] A more detailed illustration of a flash memory array 130 is provided in Figure 2. As Figure 2 illustrates, the memory cells 110 are made up of floating gate transistors 132 that are arranged in a plurality of rows and columns (only one column is illustrated in Figure 2). In the memory array, the source regions 134 of each memory cell in a row are connected to a common source line 136. The drain regions 138 of each memory cell in a column are connected to a common bit line 140. In addition, control gates 142 of each memory cell 110 in a row are connected to a word line 144. The array of Figure 2 has been simplified to illustrate the basic arrangement of memory cells and bit lines. Those skilled in the art will appreciate that the schematic diagram has been simplified to focus on the present invention and that additional rows and columns would be implemented to create a complete memory device.

[33] During an erase verify operation, a voltage is applied to word line 144 of a memory cell 110. In response to the word line voltage, the memory cell conducts a current through bit line 140. That is, the memory cell responds to the word line voltage based on a charge of floating gate 146. The level of current in the bit line indicates a state of the memory cell. That is, the memory cell may have an erase state that is either erased, over-erased or under-erased. An erase verify circuit 128, of one embodiment of the present invention, uses the bit line current to determine if memory cells are erased, over-erase or under-erased in a single step. As explained above, prior methods required a first erase verify operation to determine if memory cells are erased. A second operation is then performed to determine if memory cells were over-erased.

[34] Figure 3 illustrates a block diagram of the verify circuit 128 with a bit line input 140, two references current inputs and an output(s). The verify circuit can be selectively coupled to a bit line 140 and first and second reference currents, I_{r1} and I_{r2} . The verify circuit compares a bit line current to the two reference currents and provides an output signal that indicated if the bit line current is within a current window defined

by two reference currents. In one embodiment, the verify circuit provides multiple output signals.

[35] The verify circuit 128 can include a comparator circuit 150, as illustrated in Figure 4. The comparator circuit 150 is coupled to the bit line 140 and indicates if the bit line current (I_{bl}) is within a current window defined by the two reference currents I_{r1} and I_{r2} . The comparator circuit 150 includes first and second comparators 152, 154. The first comparator 152 compares the bit line current (I_{bl}) with the first reference current (I_{r1}) and produces a first output signal (O_{s1}). The second comparator circuit 154 compares the bit line current I_{bl} with a second reference current (I_{r2}) and produce a second output signal (O_{s2}). The two output signals can be output from verify circuit 128 or the verify circuit can use the two output signals to determine a state of the bit line current. Sample outputs of the two comparators are illustrated in Table 1.

TABLE 1

| Memory Operation | O_{s1} | O_{s2} | Memory Cell State |
|----------------------------|----------|----------|--------------------|
| $I_{bl} < I_{r1}$ | 0 | 0 | Need Further Erase |
| $I_{r1} < I_{bl} < I_{r2}$ | 1 | 0 | Pass Erase Verify |
| $I_{bl} > I_{r2}$ | 1 | 1 | Over-Erase |

[36] For example, the first reference current (I_{r1}) may be set at $50\mu A$ and the second reference current (I_{r2}) may be set at $90\mu A$. A $40\mu A$ window, therefore, is defined by these references. It should be noted that these current levels are only used as an example. The reference current levels may vary depending on defined specifications of the memory device being used. According to this example, any current over $90\mu A$ indicates that the bit line 140 is coupled to an over-erased cell and any current under $50\mu A$ indicates a current that would be found in a bit line 140 that was coupled to a memory cell 110 that was under-erased. Referring to Table 2, three possible bit line

current (I_{bl}) levels and the two output signals are illustrated when the reference currents are set at $90\mu A$ and $50\mu A$.

TABLE 2

| Bit line Current, I_{bl} | Os1 | Os2 | Memory Cell State |
|----------------------------|-----|-----|--------------------|
| 40uA | 0 | 0 | Need Further Erase |
| 70uA | 1 | 0 | Pass Erase Verify |
| 100uA | 1 | 1 | Over-Erase |

[37] Current comparators and current references of Figure 4 can be designed as shown in Figure 5, with current to voltage converters and voltage comparators. Referring to Figure 5, a comparator circuit 150 compares a bit line voltage 140 with reference voltages, V_{r1} and V_{r2} . In this embodiment, a current-to-voltage converter 160 is used to convert the bit line current to a bit line voltage (V_{bl}). The current-to-voltage converter 160 is coupled between bit line 140 and first and second voltage comparators 155, 157. A current-to-voltage converter 200 is coupled between a reference current input (I_{ref}) and first and second comparators 155, 157. Thus, the current-to-voltage converter 200 provide a first reference voltage (V_{r1}) and a second reference voltage (V_{r2}).

[38] The first comparator 155 of the comparator circuit 150 compares the bit line voltage V_{bl} with the first reference voltage V_{r1} and produces a first output signal ($Os1$). The second comparator 157 of the comparator circuit 150 compares the bit line voltage V_{bl} with the second reference voltage V_{r2} and produces a second output signal ($Os2$). An optional logic circuit 151 can be provided to process the output signals, $Os1$ and $Os2$, and provide a single output to indicate if the bit line has a voltage level within a window defined by V_{r1} and V_{r1} . The logic circuit 151 can be included with verify circuit 128. That is, the embodiments of Figures 3, 4, 5 and 6 can each comprise logic circuit 151.

[39] Figure 6 illustrates an alternate embodiment having first and second current to voltage converters 162 and 164. The first and second current-to-voltage converters provide reference voltages, V_{r1} and V_{r2} , in response to reference currents, I_{r1} and I_{r2} , respectively. Referring to Table 3, three possible bit line voltage (V_{bl}) levels and the two output signals are illustrated.

TABLE 3

| Bit Line voltage V_{bl} | Os1 | Os2 | Memory Cell State |
|----------------------------|-----|-----|--------------------|
| $V_{bl} > V_{r2}$ | 0 | 0 | Need Further Erase |
| $V_{r1} < V_{bl} < V_{r2}$ | 1 | 0 | Pass Erase Verify |
| $V_{bl} < V_{r1}$ | 1 | 1 | Over-Erase |

[40] One embodiment of bit line current-to-voltage converter 160 is illustrated in Figure 7. The bit line current-to-voltage converter 160 includes a resistor 170 and an activation circuit 172. The activation circuit 172 is used to provide a current path through the resistor. The activation circuit can include an activation transistor 174 and an inverter 182. Resistor 170 is coupled to the drain 176 of the activation transistor 174. Inverter 182 is coupled between gate 178 of the activation transistor 174 and source 180 of the activation transistor 174. In addition, source 180 of the activation transistor 174 is further coupled to bit line 140. During operation, the bit line current I_{bl} pulls the input of inverter 182 low. The inverter then activates transistor 174 to provide a current path through resistor 170. A voltage drop across the resistor establishes the bit line voltage, V_{bl} . The voltage output, V_{bl} , of the bit line current-to-voltage converter 160 can be determined by the following equation: $V_{bl} = V_{cc} - R(I_{bl})$. While this current-to-voltage converter uses the bit line current to establish the output voltage, similar converters can be used to provide reference voltages.

[44] A typical erase algorithm for a standard stacked one transistor flash cell includes three main phases: 1) pre-program to program all cells; 2) erase to apply erase pulses to the cells and verify until cells are erased; and 3) heal to detect cell leakage and apply a program scheme to over-erased cells. ^{In the} The present invention, the leakage detection step is merged with the verify portion of phase 2. As erase verification is performed, the system determines if the cell is over-erased. The cell address and status information can be latched for use in phase 3, or can be used immediately by applying the heal programming scheme to that cell, column or array.

Conclusion

[45] An erase verify system has been described that determines a state of memory cells in a non-volatile memory. The memory includes a non-volatile memory array having a plurality of memory cells coupled to bit lines. A verify circuit is coupled to the bit lines to determine if memory cells have ^{an} erase level that is within predetermined upper and lower limits. The verify circuit can include first and second comparators. The first comparator is used to compare a bit line current with an upper first reference current. The second comparator is used to compare a bit line current with a lower second reference current. The comparator circuit is not limited to reference current, but can use reference voltages and a bit line voltage. The verify circuit, therefore, eliminates the need for separate bit line leakage testing to identify over-erased memory cells. Methods of detecting a bit line current have also been described.

[46] Although specific embodiments have been illustrated and described herein, it will be appreciated by those of ordinary skill in the art that any arrangement, which is calculated to achieve the same purpose, may be substituted for the specific embodiment shown. This application is intended to cover any adaptations or variations of the present invention. Therefore, it is manifestly intended that this invention be limited only by the claims and the equivalents thereof.